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[Designing Scan Chains With Specific Parameter Sensitivities to Identify Process Defects]

Abstract

A method is disclosed for designing scan chains in an integrated circuit chip with specific parameter sensitivities to identify fabrication process defects causing test fails and chip yield loss. The composition of scan paths in the integrated circuit chip is biased to allow them to also function as on-product process monitors. The method adds grouping constraints that bias scan chains to have common latch cell usage where possible, and also biases cell routing to constrain scan chain routing to given restricted metal layers for interconnects. The method assembles a list of latch design parameters which are sensitive to process variation or integrity, and formulates a plan for scan chain design which determines the number and the length of scan chains. A model is formulated of scan chain design based upon current state of yield and process integrity, wherein certain latch designs having dominant sensitivities are chosen for specific ones of the scan chains on the chip. The model is provided as input parameters to a

global placement and wiring program used to lay out the scan chains. Test data on the chip is then analyzed to determine and isolate systematic yield problems denoted by attributes of a statistically significant failing population of a specific type of scan chain.